CLAIMS

1. A bus arbiter coupled to a first and second bus master, a first and second slave and a bus, comprising:

at least one port coupled to receive bus request commands for a transaction from either the first or second bus master and coupled to receive an address or identity of the first and second slaves for the transaction, and also coupled to communicate over the bus; and

logic circuitry that defines logic to select a bus frequency for the requested transaction.

2. The bus arbiter of claim 1 wherein the logic circuitry defines logic to select a bus frequency according to the identity of the slave for the requested transaction.

3. The bus arbiter of claim 1 wherein the logic circuitry defines logic to select a bus frequency according to the identity of the master for the requested transaction.

4. The bus arbiter of claim 1 wherein the logic circuitry defines logic to select a bus frequency according to the length of the bus between the first or second master and the first or second slave according to which ones are involved in the requested transaction.

5. A method for generating sample cycle pulses, comprising:

determining a ratio of an internal clock to the clock of a bus; and

generating a sample cycle pulse in an appropriate cycle of the internal or faster clock.

6. The method of claim 5 wherein the ratio of clocks is determined by counting the negative or falling edges of the faster clock pulses in two periods of the slower clock and divide that by 2.

7. A method for communicating over a bus, comprising:

generating a request for access or control of the bus, which request is generated by a bus master;

determining a bus frequency being set by the bus arbiter;

receiving a grant from the bus arbiter indicating that the bus master may take control of the bus;

commencing a transaction at a frequency that matches the bus frequency;

comparing an internal clock frequency to the frequency of the bus;

generating internal sample cycle signals;

whenever a sample cycle signal is generated, latching data on the bus; and

upon termination of the transaction, issuing a release signal to release the bus to the next master waiting for bus resources.

8. The method of claim 7 wherein the relative difference between the internal clock frequency and the bus clock frequency is determined by counting falling edges of the clock cycles for the internal clock in two periods of the bus clock.

9. The method of claim 7 wherein the data is latched while the sample signal is high and wherein data is written or "driven" right after the sample signal goes low.

10. A method for selecting a bus frequency, comprising:

setting a bus frequency according to the identity of the devices that will be a part of the transaction; and

setting a bus frequency so that any receiver for the communications of the transaction will have a frequency that is an integer multiple of the bus frequency.

11. The method of claim 10 further comprising the step of determining the identity of a master bus and its corresponding internal frequency.

12. The method of claim 10 further comprising the step of determining the identity and corresponding internal frequency of a slave or receiver device.

13. The method of claim 10 further comprising the steps of determining the identity of the devices in the transaction and examining a table to determine a corresponding bus frequency.

14. The method of claim 10 wherein the bus frequency for the transaction is determined dynamically rather than by performing a table lookup.

15. The method of claim 10 wherein the bus frequency also is set according to an expected or determined amount of impedance in the bus between the terminals that are a part of the transaction.

16. The method of claim 10 wherein the bus frequency is determined by a bus arbiter.

17. The method of claim 10 wherein the bus frequency is determined by a clock generation controller.

18. The method of claim 10 wherein the frequency of the bus is determined by a bus master.

19. A bus slave, comprising:

at least one input port for receiving communication signals and control signals;

circuitry for determining a bus frequency;

circuitry for determining a ratio between an internal

clock of the bus slave and the bus frequency; and

circuitry for determining when to latch communication signals being received over the at least one input port.

20. The bus slave of claim 19 further including a state machine for generating a sample cycle signal, the sample cycle signal for prompting the slave to latch the communication signals as a part of determining when to latch communication signals.